

## JERRY A. WITTMANN

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### SUMMARY

Senior Electrical Engineer, with broad experience in ASIC and Microcontrollers for Bipolar, CMOS, and BiCMOS Semiconductor technologies. Expertise in Device, Process, Product, Project, Reliability, Quality Assurance and Test Engineering. Additional experience in all current flip chip, bump and packaging technologies including multichip and microwave modules. Strong educational credentials, fluent in the German language. Strengths include:

- System & Device Integration
- Developmental Management
- Yield Enhancement on Processes
- Wafer & Assembly Mfg
- Prototyping / NPD
- ISO / QS9000 / 6 Sigma
- Communication Skills
- Failure Analysis & DFM
- Defect Reduction

### PROFESSIONAL EXPERIENCE

#### **ST. JUDE MEDICAL – Cardiac Rhythm Management Division, Scottsdale Arizona 2001-2007**

##### Staff Project Leader for Wafer Yield Improvement Activities Engineer/Scientist

Project Leader for Wafer Yield Improvement Projects. Worked with wafer foundry suppliers such as AMI, UMC, Supertex. Interfaced with all engineering disciplines such as Device, Process, Product, Quality, and Design Engineering Groups at SJM and Wafer foundry suppliers.

- Responsible for driving wafer yield improvement on custom analog and Digital ASIC's. Directed a line down situation from 0% to a stable 80% wafer yield in a short four-month timeframe. This wafer process fix resulted in 1.12 M yearly sustained cost savings.
- Responsible for driving all aspects of failure analysis and root cause corrective action activities for ASIC's in production and field return devices. Familiar with all failure analysis techniques such as SEM, EDX, Liquid Crystal and EMMI.

#### **MOTOROLA / ON Semiconductor – Chandler, Mesa, Phoenix, Scottsdale Arizona 1981-2001**

##### Staff Program Manager New Product Development Engineer/Scientist

2000 – 2001

Program Manager for managing, scheduling and implementing new product development and process optimization experiments for Power MOS devices. Worked closely with Product, Design, QA, Process, and wafer fabrication/assembly manufacturing personnel to institute qualification acceptance and process stability.

##### Staff Product Engineer/Scientist

1998 – 2000

Project leader for managing, scheduling and implementing new product development and process optimization experiments for multiple 5" & 8" wafer level burn-in (WLBI) flip chip programs. Worked closely with Product, Design, QA, Process, Manufacturing and customers to institute qualification acceptance and process stability.

Staff Reliability and Quality Assurance Engineer/Scientist

1994 – 1998

Managed and led process and defectivity enhancement programs for Bipolar CMOS, BiCMOS technologies for Microcontrollers and ASIC devices, utilizing IDR and UDR design rules.

- Determined root cause corrective actions for wafer and flip chip defectivity issues, resulting in yield improvements of up to 10%. Led cross-functional teams to analyze and resolve external and internal customer returns using the 8D approach.
- Chaired operation of Process Change Review Boards, Material Review Boards, and all Reliability issues. Instrumental in increasing yield, reducing cycle time and lowering production costs.
- Developed, implemented, and managed internal audit program resulting in business unit obtaining QS9000 certification. Included complete system implementation of process audits, such as: tree diagram checklists, audit reports, corrective action responses, escalation procedures and scheduling

Staff ASIC Reliability Engineer

1991 – 1994

Researched, analyzed and implemented solutions for process technology problems in Bipolar and CMOS wafer fabrication facilities as a member of process and yield improvement teams. Performed ASIC product and qualification reliability stress testing for multiple wafer fabrication facilities. Characterized and qualified new product designs of silicon wafers, die, and plastic/ceramic IC packaging.

Senior Project Manager

1990 – 1991

Managed and directed a project team of four product/device engineers, seven technicians, and two material specialists for a \$1.5M classified aerospace program.

- Performed management and technical support duties for high reliability integrated circuit and electronic system builds for the electronic government and military customers. Projects responsibilities included: management of all project activities, project scheduling and timelines, daily & weekly progress reporting to internal and external customers, budgets, and purchasing and proposal generation. Project was successful, resulting in a 25% reduction in the total project cost.

Senior Project Leader & Test Engineer

1981 – 1990

Performed qualification and product/device development for high reliability builds. Led all technical aspects of project utilizing cross-functional teams. Served as technical liaison with prime contractors as well.

- Piloted new microwave FET designs into a production environment, optimizing design layout and performance characteristics, resulting in a \$75K cost savings. Implemented new frequency encoder ASIC designs into a production environment, which resulted in a 50% reduction in cycle time.
- Analyzed critical field failure for the NASA space shuttle program. Utilized circuit design/layout analysis, reverse engineering techniques including Calma design tools, schematic capture, SEM analysis, and voltage contrast. Achieved a sound redesign that was integrated into the system with minimal impact to the critical launch date requirements.

**EDUCATION/PROFESSIONAL DEVELOPMENT**

Masters of Science: Electrical Engineering, course work completed, thesis required.

Bachelor of Science: Electrical Engineering, Honors Graduate, Arizona State University, Tempe, Arizona

Continuing Education: Statistical Process Control, Cycle Time Management, Annual Reliability Physics Symposium, Leadership/Management Development Seminar, ISO, QS9000, & 6 Sigma Black Belt Training and Certification. Published Article at ESD Symposium on Custom CMOS LSI device.